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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,283	04/30/2001	Aaron Buchwald	1875.0560003	1013

28393 7590 05/05/2005	EXAMINER
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVE., N.W. WASHINGTON, DC 20005	ZHENG, EVA Y

ART UNIT	PAPER NUMBER
2634	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/844,283	BUCHWALD ET AL.
	Examiner	Art Unit
	Eva Yi Zheng	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☒ This action is **FINAL.** 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11,13-19 and 21* is/are rejected.

7)☒ Claim(s) *5-10,20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed Dec 28, 2004 have been fully considered but they
are not persuasive. Applicant's amendment necessitated the new ground(s) of
rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL.
The Examiner has thoroughly reviewed Applicant's arguments but firmly believes that
the cited reference reasonably and properly meet the claimed limitation as rejected.

a)   Applicant's argument – Regarding claim 1, Dabell does not teach, "performing
an equalizing process on the analog samples".

        Examiner's response – It is well known and obvious to one of ordinary skill in the
art to realize whether equalizing on the analog samples or digital samples is merely a
matter of design choice. Please refer to 35 U.S.C 103 (a) rejection in the office action
below.

b)   Applicant's argument – Regarding claims 13 and 14, Dabell failed to teach,
"equalizing time staggered portions" of a single or a plurality of multi-gigabit analog
signals.

        Examiner's response – Regarding claim 13 and 14, Dabell discloses

        (1) sampling a multi-gigabit analog information signal at a plurality of phases
(141-144 in Fig. 1, Col 3, L 6-9; 220 in Fig. 2, Col 3, L 24-27);

        (2) measuring an equalizing quality of the samples from one of the plurality of
phases (Fig. 4);

(3) equalizing the samples from each of the phases based on the measured

equalization quality of the one phases (330 in Fig. 3); and

(4) quantizing the equalized samples (351-354 in Fig. 3).

All of these features constitute equalizing time staggered portions.

c)   Applicant's argument – Regarding claim 15, Dabell failed to teach, "generating a

clock signal for each of the multi-gigabit analog information signals from each of the

respective multi-gigabit analog information signals".

Examiner's response – Although Dabell did not specifically show a clock signal in

drawing, it is well known that an equalizer comprises a clock signal and it has direct

relationship with sampling in DSP. In other words, a circuit for maintaining proper

sampling timing, the main channel equalizer error is correlated with a derivative channel

signal to derive a clock correction signal. Therefore, the equalizer by Dabell must

contain a clock signal in order for proper sampling.

d)   Applicant's argument – Regarding claim 16, Dabell failed to teach, "minimize

intersymbol interference in samples".

Examiner's response – Dabell discloses an equalization monitor in details as

shown in Fig. 6, wherein a Viterbi error detection/correction circuit 630 is used to detect

errors and applies to a comparator with a tolerable bit error rate stored. It is well known

that the practice to minimize the effect of intersymbol interference by channel

equalization is to adjusts the pulse shape so that it does not interfere with neighboring

pulses at pulse centers. Viterbi error detection/correction is error detection and

correction algorithm to clean up the received data. Therefore, Dabell did not fail to teach minimize intersymbol interference in samples.

e)   Applicant's argument – Regarding claim 21, Shimomura failed to teach, "interface board including a plurality of receivers coupled to said backplane signals, each said receiver including an adaptive equalizer".

Examiner's response – Shimomura et al. disclose a system comprising:

a backplane (18 in Fig. 1) having a plurality of signal paths (λ1-n in Fig.1); and

at least one interface coupler (12 in Fig. 1) coupled to said backplane, said interface board including a plurality of receivers (13-n in Fig. 1) coupled to said backplane signal paths, each said receiver including an adaptive equalizer (inherent as 14 in Fig. 1);

wherein each said equalizer adapts to an associated backplane signal path to equalize an signal received from said associated backplane signal path (as shown in Fig. 1).

Shimomura et al. disclose all the subject matter described above except for the specific teaching of an interface board coupled to the backplane. Instead, Shimomura et al. disclose optical coupler coupled to the backplane.

However, it is a common knowledge that an electrical signal router comprises interface board. In optical signal system coupler replaces an interface board. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to realize that different signal system comprise different interface technology,

although their functionalities are essentially the same. It would have been designer's

choice merely base on signal source.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1-3, 11 and 13-19 are rejected under 35 U.S.C. 103(a) as being

anticipated by Dabell (US 6,62,862 B1).

a)   Regarding claim 1, Dabell discloses a method for adaptively equalizing a multi-

gigabit analog information signal for a signal path, comprising the steps of:

(1) sampling a multi-gigabit analog information signal (141-144 in Fig. 1, Col 3, L

6-9; 220 in Fig. 2, Col 3, L 24-27);

(2) performing an equalizing process on the samples (330 in Fig. 3); and

(3) quantizing the equalized samples of the multi-gigabit analog information

signal (351-354 in Fig. 3).

Dabell discloses all the subject matters described above except for the specific

teaching of performing an equalizing process on the analog samples. However, such

limitations are merely a matter of design choice and would have been obvious in the

system of Dabell. Dabell teaches an equalization controller from an analog to digital

converted input, apply its output to a quantizer and generation a digital signal output.

Current application discloses an analog input applies to an equalizer and then to a

quantizer and generation a digital signal output (as shown in Fig. 2 and specification).

The location/step of where to convert analog signal into digital signal for the invention as

a whole and presents no new or unexpected results, as long as the analog signal has

been sampled, equalized and quantized. Therefore, to have equalizer analog signal in

Dabell would have been mater of obvious design choice to one of ordinary skill in the

art.

b)   Regarding claim 13, Dabell discloses a method for adaptively equalizing time

staggered portions of a multi-gigabit analog information signal for a signal path,

comprising the steps of:

        (1) sampling a multi-gigabit analog information signal at a plurality of phases

(141-144 in Fig. 1, Col 3, L 6-9; 220 in Fig. 2, Col 3, L 24-27);

        (2) measuring an equalizing quality of the samples from one of the plurality of

phases (Fig. 4);

        (3) equalizing the samples from each of the phases based on the measured

equalization quality of the one phases (330 in Fig. 3); and

        (4) quantizing the equalized samples (351-354 in Fig. 3).

c)   Regarding claim 14, Dabell discloses a method for adaptively equalizing a time

staggered portions of a plurality of multi-gigabit analog information signals for respective

signal paths, comprising the steps of:

(1) generating clock signals from the plurality multi-gigabit analog information

signals (141-144 in Fig. 1, Col 3, L 6-9);

(2) sampling each of the multi-gigabit analog information signals at a plurality of

phases of the respective clock signals (220 in Fig. 2, Col 3, L 24-27);

(3) measuring an equalization quality of the samples from one of the plurality of

phases for each of the multi-gigabit analog information signals (as shown in Fig. 4);

(4) equalizing the samples from each of the phases of each of the multi-gigabit

analog information signals based on the measured equalization quality of the one phase

of each of the respective multi-gigabit analog information signals (330 in Fig. 3); and

(5) quantizing the equalized samples (351-354 in Fig. 3).

d)   Regarding claim 15, Dabell discloses a method for adaptively equalizing a

plurality of multi-gigabit analog information signals for respective signal paths,

comprising the steps of:

(1) generating a clock signal for each of the multi-gigabit analog information

signals from each of the respective multi-gigabit analog information signals (141-144 in

Fig. 1, Col 3, L 6-9);

(2) sampling each of the multi-gigabit analog information signals according to the

respective clock signals (220 in Fig. 2, Col 3, L 24-27);

(3) performing an equalizing process on the samples (330 in Fig. 3); and

(4) quantizing the equalized samples (351-354 in Fig. 3).

e)   Regarding claim 16, Dabell discloses a system for quantizing a multi-gigabit

analog information signal, comprising:

(1) a sampler (220 in Fig. 2);

(2) an equalizer coupled to said sampler (150 as shown in Fig. 3); and

(3) a quantizer coupled to said equalizer (351-354 in Fig. 3);

wherein said equalizer minimize inter-symbol interferences in samples output

from said sampler and said quantizer quantizes equalized samples output from said

equalizer (Col 3, L 55-Col 4, L30).

f)   Regarding claim 2, Dabell discloses the method according to claim 1, wherein

step (2) comprises the steps of:

(a) comparing a multi-level representation of the equalized samples with the

quantized equalized samples (640 in Fig. 6, Col 4, L 67 – Col 5, L9);

(b) performing a least-means-squared operation on results of the comparison

(440 in Fig. 4, Col 4, L 8-11);

(c) adjusting an equalization coefficient with a result of the least-means-squared

operation (Col 4, L 14-27); and

(d) repeating steps (2)(a) through (2)(c) (as shown in Fig. 4).

g)   Regarding claim 11, Dabell discloses the method according to claim 1, wherein

step (2) comprises the step of minimizing inter-symbol interferences in the samples (as

shown in Fig. 4; Col 4, L 4-18).

h)   Regarding claim 12, Dabell discloses the method according to claim 1, wherein

step (2) comprises the step of minimizing inter-symbol interferences in the samples (as

shown in Fig. 4; Col 4, L 4-18).

i)   Regarding claim 17, Dabell discloses the system according to claim 16, wherein said equalizer comprises an finite impulse response filter ("FIR") (341-344 in Fig. 3) having at least one adjustable tap (as shown in Fig. 5), said system further comprising control logic coupled to said FIR (330 in Fig. 3), wherein said control logic generates tap updates for said FIR (440 in Fig. 4).

j)   Regarding claim 18, Dabell discloses the system according to claim 17, wherein said control logic comprises:

a first input (141-144 in Fig. 3) coupled to an output of said equalizer (as shown in Fig. 3);

an analog-to-digital converter ("ADC") (321-324 in Fig. 3) coupled to said first input (141-144 in Fig. 3); and

a control module (330 in Fig. 3) coupled to an output of said ADC;

wherein said ADC generates multi-level representations of equalized samples (Col 3, L39-45), and said control module generates said tap updates from at least said multi-level representations of the equalized samples (440 in Fig. 4).

k)   Regarding claim 19. Dabell discloses the system according to claim 17, wherein said control logic comprises:

a second input (301-301 in Fig. 3) coupled to an output of said quantizer (as shown in Fig. 3); and

a least-means-squared ("LMS") module coupled to said first and second control logic inputs (Fig. 4);

wherein said LMS module compares the multi-level representations of equalized samples with the quantized samples from said quantizer and generates said tap updates according to the comparison (Col 4, L 8-25).

I)   Regarding claim 3, Dabell discloses all the subject matters described above except for the specific teaching of equalizing process has a sub-sampling rate relative to the sampling rate of analog information signal.

However, it is well known and common knowledge that the equalizer sampling rate is not same as the input signal sampling rate due to tap coefficient in equalization control (as shown in Fig. 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to conclude that the sampling rate of equalizer by Dabell is a sub-sampling rate relative to the input signal.

4.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dabell (US 6,62,862 B1) in view of applicant admitted prior art.

Regarding claim 4, Dabell discloses all the subject matters described above except for the specific teaching of equalizer process at an off-set of a sub-sampling rate relative to the sampling rate of analog information signal.

However, it is well known and common knowledge that ADC can operated on every equalized sample from the FIR filter, or any subset and or off-set thereof (Pg 6, [0144]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to conclude that the equalizer system by Dabell performs at an off-set of a sub-sampling rate relative to the input signal.

5.   Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Shimomura et al. (US 6,404,525 B1).

Regarding claim 21, Shimomura et al. disclose a system for routing and

adaptively equalizing high data rate analog data signals, comprising:

a backplane (18 in Fig. 1) having a plurality of signal paths (λ1-n in Fig.1); and

at least one interface coupler (12 in Fig. 1) coupled to said backplane, said

interface board including a plurality of receivers (13-n in Fig. 1) coupled to said

backplane signal paths, each said receiver including an adaptive equalizer (inherent as

14 in Fig. 1);

wherein each said equalizer adapts to an associated backplane signal path to

equalize an signal received from said associated backplane signal path (as shown in

Fig. 1).

Shimomura et al. disclose all the subject matter described above except for the

specific teaching of an interface board coupled to the backplane. Instead, Shimomura

et al. disclose optical coupler coupled to the backplane.

However, it is a common knowledge that an electrical signal router comprises

interface board. In optical signal system coupler replaces an interface board. Therefore,

it would have been obvious to one of ordinary skill in the art at the time of invention was

made to realize that different signal system comprise different interface technology,

although their functionalities are essentially the same. It would have been designer's

choice merely base on signal source.

Allowable Subject Matter

6.   Claims 5-10 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Yi Zheng whose telephone number is (571) 272-3049. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number

for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal

Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the Technology Center 2600 Customer Service Office

whose telephone number is (703) 306-0377.

Eva Yi Zheng
Examiner
Art Unit 2634

April 22, 2005

SHUWANG LIU
PRIMARY EXAMINER